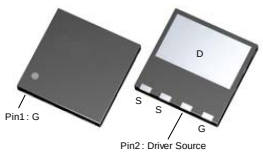
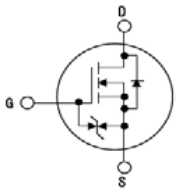
650V N-Channel Super Junction MOSFET

Features

- BV_{DSS}=650 V, I_D=6.7 A
- $R_{DS(on)}$:0.64Ω (Max) @ V_{GS}=10V
- Very Low FOM ($R_{DS(on)}$ X Q_g)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode



DFN8x8



Application

- Switch Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power
- AC to DC Converters
- Telecom

RoHS

Device Marking and Package Information

Ordering Code	Package	Marking
MPSY65M640B	DFN8x8	MP65M640B

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current - Continuous (T_C = 25℃)	6.7 *	A
	Drain Current - Continuous (T_C = 100℃)	4.2 *	A
I_{DM}[1)]	Drain Current - Pulsed	20 *	A
E_{AS}[2)]	Single Pulsed Avalanche Energy	73	mJ
I_{AR}	Avalanche Current	1.3	A
dv/dt	MOSFET dv/dt ruggedness, VDS=0…400V	50	V/ns
dv/dt	Reverse diode dv/dt, V_{DS}=0…400V, I_{DS}≤I_D	15	V/ns
P_D	Power Dissipation (T_C = 25℃)	63	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

* Drain current limited by maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.98	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient , Max.	62.5	℃/W

Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 220 μA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.0 A	-	0.555	0.64	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1mA	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0	-	-	1	μA
		V_{DS} = 650 V, T_C = 150℃	-	-	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1.0 MHz	-	588	-	pF
C_{oss}	Output Capacitance		-	17	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.7	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 325 V, I_D = 2.9 A, R_G = 25 Ω (Note 3,4)	-	23	-	ns
t_r	Turn-On Rise Time		-	18	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	77	-	ns
t_f	Turn-Off Fall Time		-	18	-	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 2.9 A, V_{GS} = 10 V (Note 3,4)	-	14	-	nC
Q_{gs}	Gate-Source Charge		-	2.6	-	nC
Q_{gd}	Gate-Drain Charge		-	4.5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	6.7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	20	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.9 A	-	-	1.3	V
trr	Reverse Recovery Time	V_R = 400 V, I_F = 2.9 A, di_F/dt = 100 A/μs	-	250	-	ns
Qrr	Reverse Recovery Charge		-	1.8	-	μC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=1.3A V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
4. Essentially Independent of Operating Temperature

Typical Characteristics

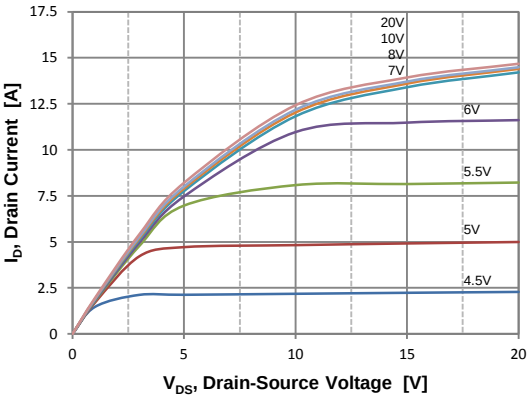


Figure 1. On Region Characteristics

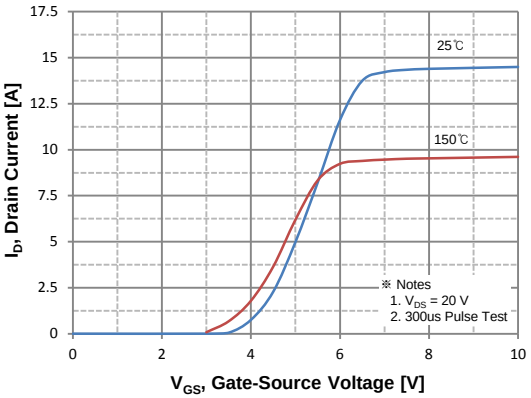


Figure 2. Transfer Characteristics

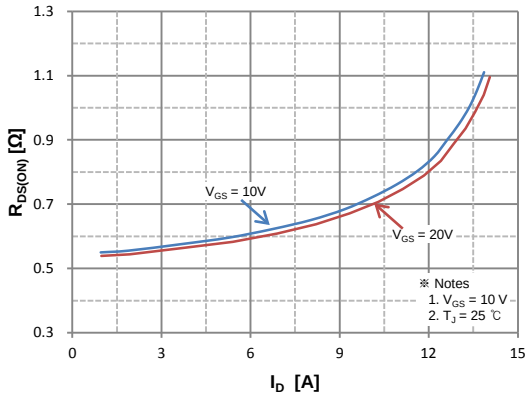


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

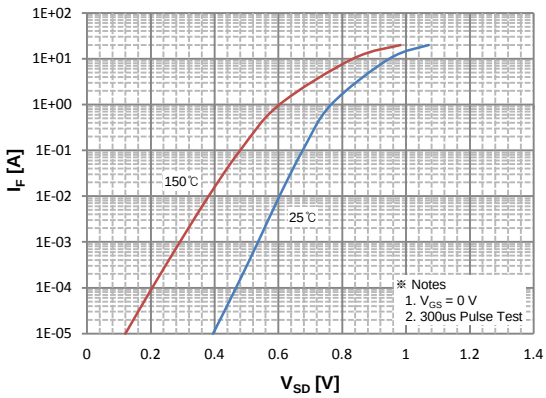


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

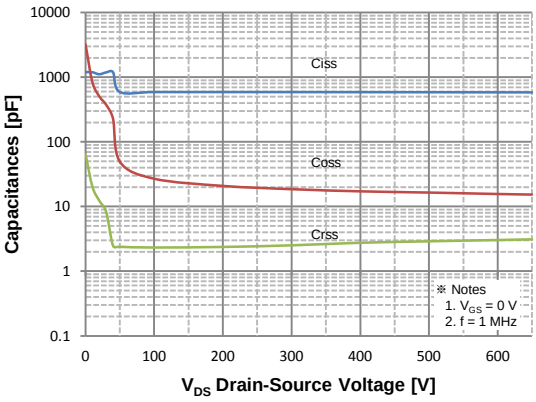


Figure 5. Capacitance Characteristics

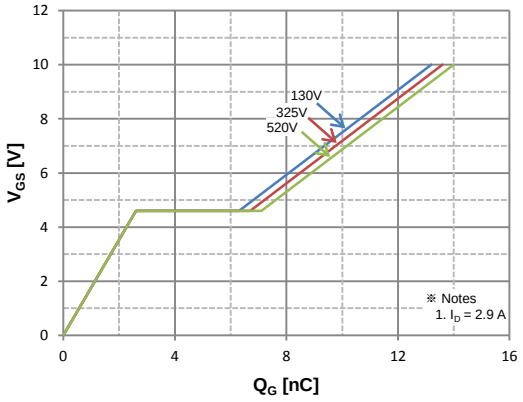


Figure 6. Gate Charge Characteristics

Typical Characteristics

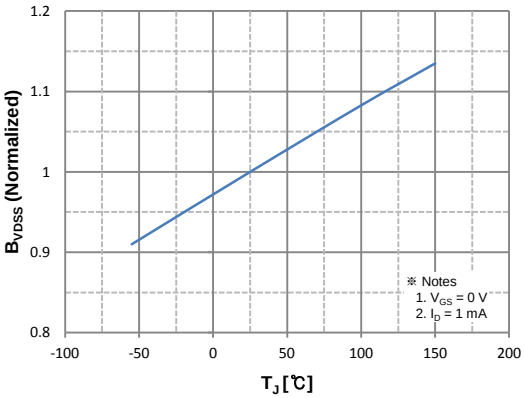


Figure 7. Breakdown Voltage Variation vs. Temperature

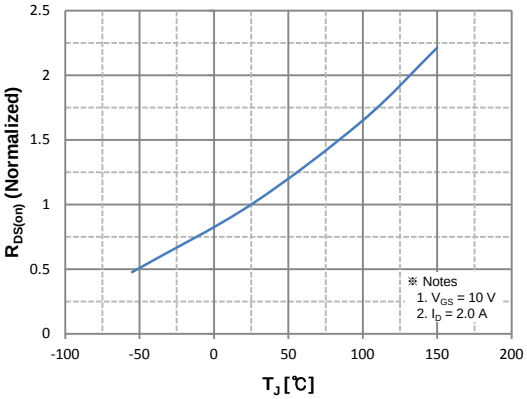


Figure 8. On-Resistance Variation vs. Temperature

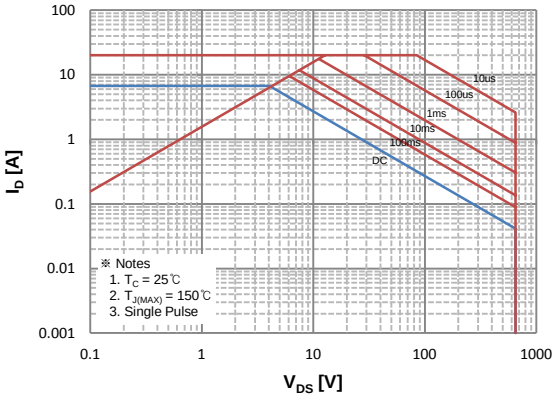


Figure 9. Maximum Safe Operating Area

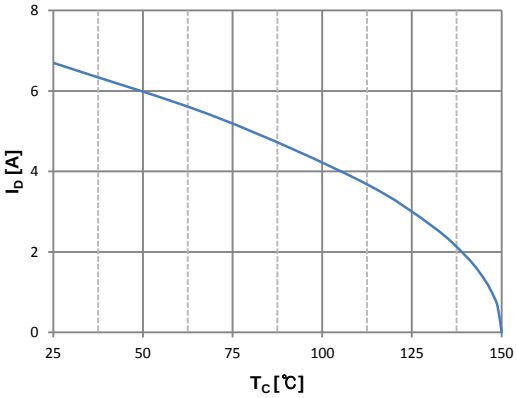


Figure 10. Maximum Drain Current vs. Case Temperature

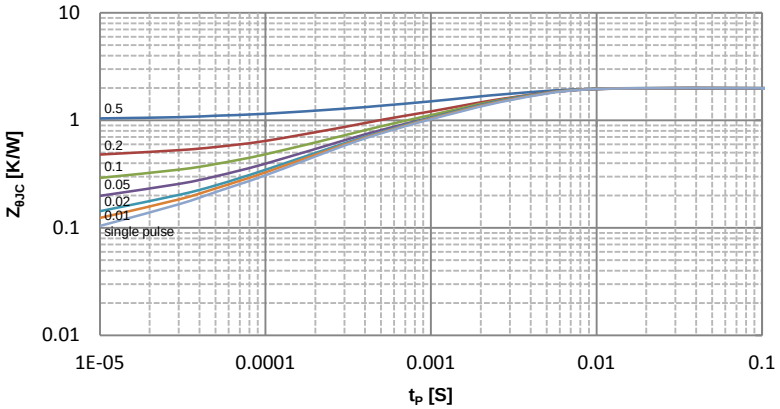


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

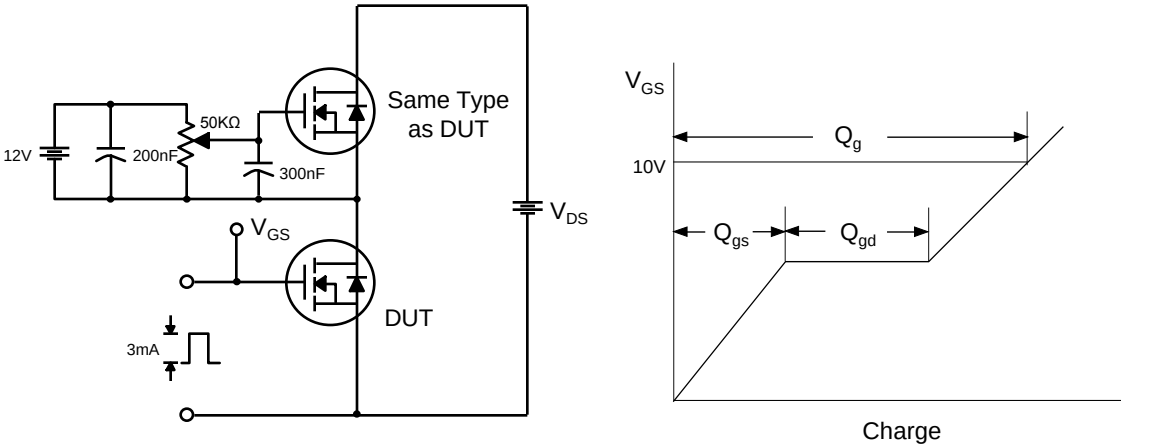


Fig 13. Resistive Switching Test Circuit & Waveforms

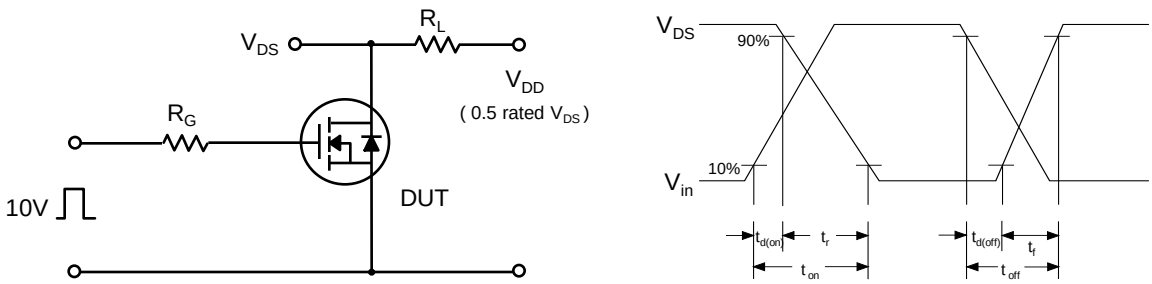


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

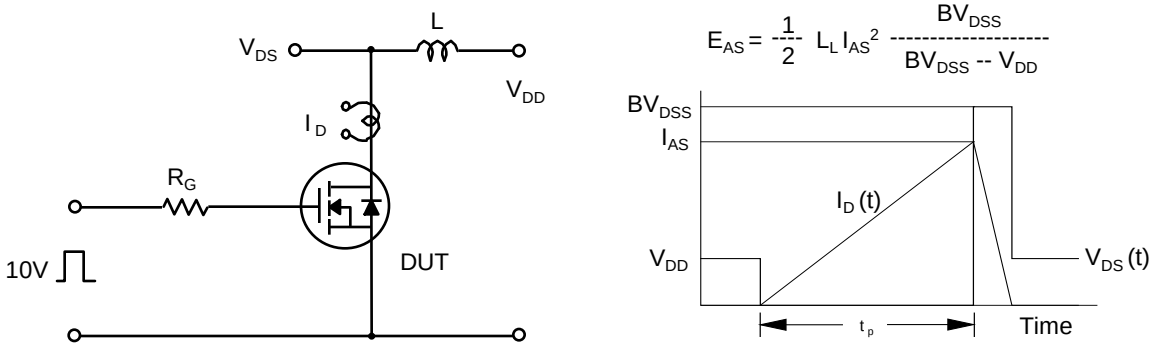
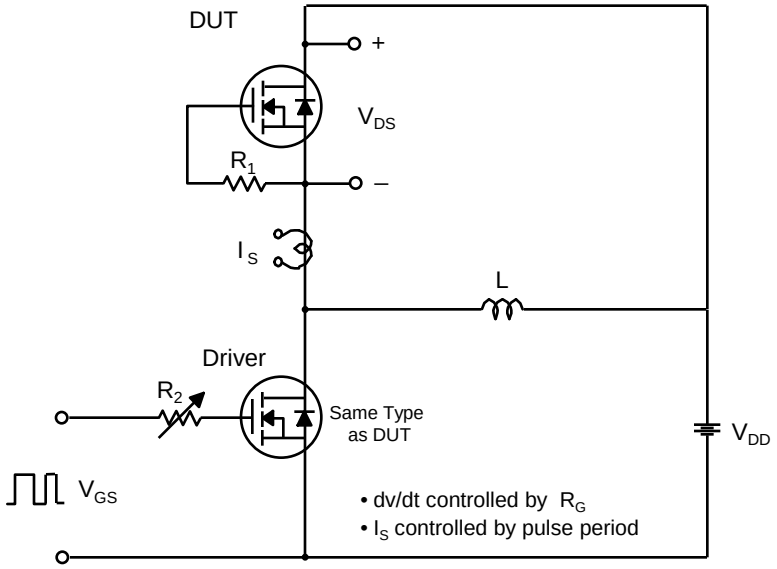
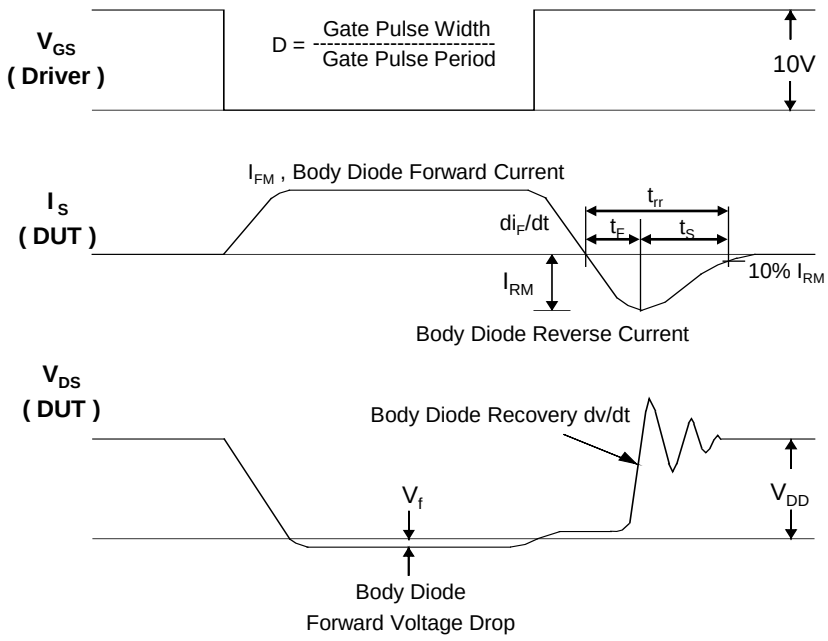


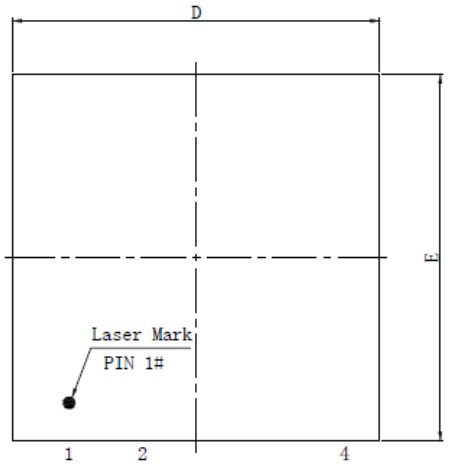
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



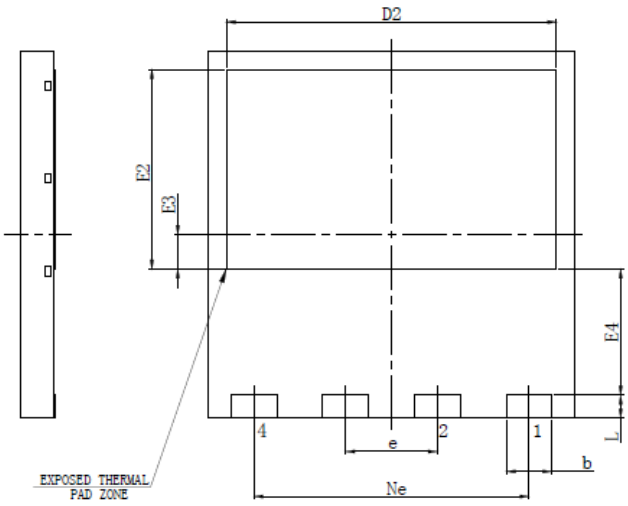


Package Dimension

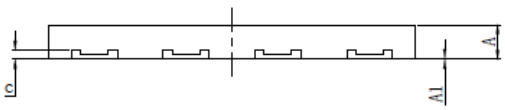
DFN 8x8



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.95	1.00	1.05
c	0.18	0.20	0.25
D	7.90	8.00	8.10
Ne	6.00BSC		
e	2.00BSC		
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E2	4.25	4.35	4.45
E3	0.75REF		
E4	2.75REF		
L	0.45	0.50	0.55
载体尺寸	7.60*5.15		